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Design and Analysis of Low Power High Speed Full Adder Cell using Modified GDI Technique at 90nm Technology

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Abstract: Full adder circuit is a very important component in the design of application of integrated circuits in VLSI. This paper explores the design and analysis of four different 1 bit Full Adder cell using the Modified Gate Diffusion Input (MGDI) technique on optimizing the power, delay and Power Delay Product (PDP). This technique (MGDI) allows reducing power, delay and area of digital circuits, while maintaining low complexity of logic design. Through investigation is carried out for the effectiveness using combination of different low power full adder circuit design techniques. The main objective of these full adders is providing high-speed and low power consumption also provides good voltage swing. This can be achieved by applying the low power techniques for reduction of power and delay. This work presents comparison of the different low power full adder cell on the power dissipation, delay and Power delay product. The full adder design simulations are implemented using 90nm technology with Tanner EDA Tool.

Keywords: Full Adder, GDI, MGDI, Power, Delay, PDP.

1. INTRODUCTION

Full adders are fundamental circuits used for performing arithmetic operations. Multipliers, subtraction, comparators, and address calculation are some of the well known operation based on addition. These operations are mostly used in VLSI applications. One of the most important issues in VLSI design application is power consumption, area and speed. With the continuously increasing chip complexity and increasing transistors number in a chip, circuit power consumption is increases as well. Therefore, reducing power consumption in full adders, it will reduce the all power consumption of the whole system. Most of the VLSI applications, such as image processing, video processing, DSP and microprocessors mostly used arithmetic operation. Designing of low power and high speed VLSI system has emerged as highly popular because of the fast growing technologies in mobile and other battery power applications. Here different design full adder styles have been proposed to implement 1-bit adder cell, these adder cells commonly aimed to reduce the power consumption, area, delay and increase speed.

Complementary CMOS [1, 2, 3] full adder is based on the NMOS pull down and PMOS pull up transistors. This full adder circuit provides full swing which is most important when utilized in a more complex structure. The layout of the C-CMOS full adder is very simple and efficient due to the complementary transistor pairs used for designing circuit structure, however due to used the large number of PMOS transistors in its structure so its directly effect on the area. A Complementary Pass Transistor Logic (CPL) full adder [1, 2, 3] is a dual-rail structure with 32 transistors. It provides full swing output and good driving capability at high speed due to the fast differential stage of cross-coupled PMOS transistors. The main issue of CPL is large power consumption due to increase the number of internal nodes and static inverters. The existing internal node and inverters are the primary source of the static power dissipation and leakage current.

Transmission Function Full Adder (TFA) [3, 4, 5] and Transmission Gate Full Adder (TGA) [3, 5] designs are low power consuming and no voltage drop problem. These circuit designing is suitable for XOR/XNOR gates. The main drawback of this adder design is double number of transistor to design a similar function and lack driving capability. The TFA or TGA full adders are cascaded then there performance degrades. Hence for improving the weak driving capability required the additional buffer, but additional buffer increase the chip size area and increasing the power consumption.

In this paper, four different 1-bit full adder designs are simulated and analysed using the modified GDI technique. The designs are- 12T MGDI, full adder, 10T MGDI, full adder, 9T MGDI full adder and 8T MGDI full adder. These four full adder cell designs are compared based on the power dissipation, propagation delay and PDP

2. GDI CELL TECHNIQUE

GDI [8, 9, 10] technique is design for low power digital circuit which allows minimum chip area, delay and low power consumption. GDI method is based on the use of a simple cell as shown in Fig. 1. The Truth Table of the GDI

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cell is shown in Table. 1. GDI technique allows implementation of complex logic functions using only two transistors over a wide range application. The GDI basic cell is similar to the standard CMOS inverter but it is connected to the two terminal N and P, so it can be randomly biased at contrast with CMOS inverter. The major difference between GDI and CMOS is the designing of circuit as in GDI the source of the PMOS transistor is not connected to VDD and the source of the NMOS is not connected to ground. Due to this important change in the design, GDI based circuits have two extra input pins.

Table 1 Truth table of the basic GDI Cell

N	P	G	OUTPUT	FUNCTION
0	1	A	$\bar{A}$	INVERTER
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{A}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}B$+AC	MUX

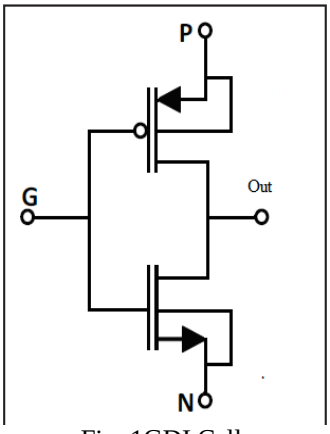

Fig. 1GDI Cell

The GDI design is more flexible as compared to the CMOS design. GDI cell have three inputs. The first input G is the common gate input of NMOS and PMOS transistors, second input P is connect to the source/drain of PMOS transistor and the last input N is connected to the source/drain of NMOS transistor. Bulk of NMOS transistor is connected to the input terminal N and bulk of PMOS transistor is connected to the input terminal P. The main issue with GDI is due to the requirement of the twin-well CMOS or silicon on insulator (SOI) process to realize. When these issues occur it will be more expensive to realize a GDI chip. Another factor with GDI that it will face the problem of lacking driving capability due to the use of standard p-well CMOS process which makes it more expensive and difficult to realize as a feasible chip.

3. MODIFIED GDI CELL

The basic cell of Modified GDI [12, 14] is similar to that of GDI Cell. The main difference between GDI and Modified GDI cell is that the bulk or body of PMOS transistor is connected to the V_{DD} and the bulk or body of NMOS transistor connected to the ground in modified GDI. Whereas in GDI Cell, body of the PMOS is connected to the drain and body of NMOS is connected to source. The basic circuit of Modified GDI cell show in the fig. 2. The Modified GDI logic style provides a low power and area efficient logic styles, which is implementable in all current CMOS transistor fabrication technologies. This make the GDI to constant body biasing in modified GDI Cell which in turn grow up the stability of the circuit and its loading effect. This exceptional arrangement of Modified GDI cell provides considerable reduction of both sub-threshold and gate leakage. Modified GDI is quite suitable for design of high speed low power circuits, and broad range of other logic circuit as it offer less number of transistors, even as improving static power characteristics and swing degradation, and allowing easy top-down design by using a small cell library.

Table. 2. Truth Table of Modified GDI Cell

N	Sn	P	Sp	G	OUTPUT	FUNCTION
0	0	1	1	A	$\bar{A}$	INVERTER
0	0	B	1	A	$\bar{A}B$	F1
B	0	1	1	A	$\bar{A}$+B	F2
1	0	B	1	A	A+B	OR
B	0	0	1	A	AB	AND
C	0	B	1	A	$\bar{A}B$+AC	MUX

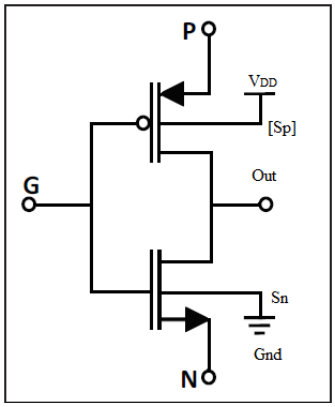

Fig. 2. Modified GDI Cell

4. MODIFIED GDI FULL ADDER

A. 12T MGDI Full Adder

The 12T Modified GDI full adder design cell eliminating the need for complicated XOR-XNOR gates, it is also implementation of this Ultra Low Power circuit using modified GDI technique. By considering the full adder's figure, it can be seen that C_{out} is equal to the output of AND gate (A AND B) when C_{in} equal to the zero, and C_{out} is equal to the output of OR gate (A OR B) when C_{in} equal to the one. Thus a multiplexer can be used to obtain the C_{out} output. Following the same process, the SUM output is equal to the output of the OR gate (A OR B OR C_{in}) when C_{out} is equal to the zero, and SUM is equal to the

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output of the AND gate (A AND B AND C_{in}) when C_{out} is equal to the one. Hence, an alternative logic design of a full adder cell can be formed by AND, OR and MUX logic blocks as shown in Fig. 3. The Modified GDI full adder provides the low power high speed with good voltage swing.

B. 10T MGDI Full Adder

This full adder design is implemented using the XOR/XNOR gate. XOR gate function is the key variable in adder equations. If the generation of XOR functionality is optimized, it can greatly enhance the performance of the full adder cell.

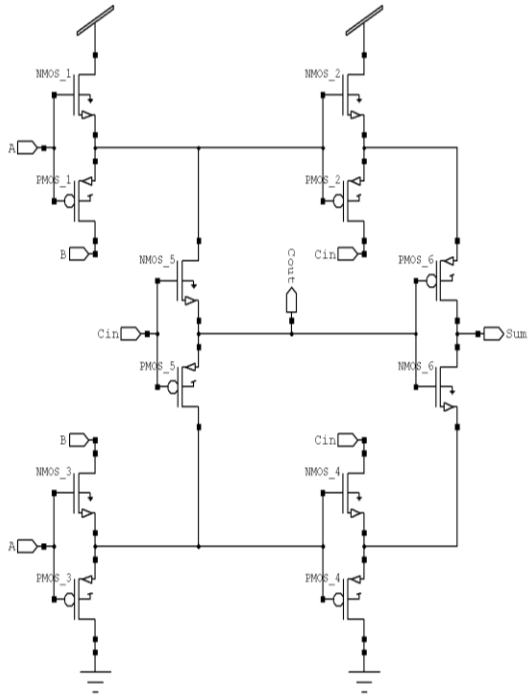

Fig. 3. 12T MGDI Full Adder

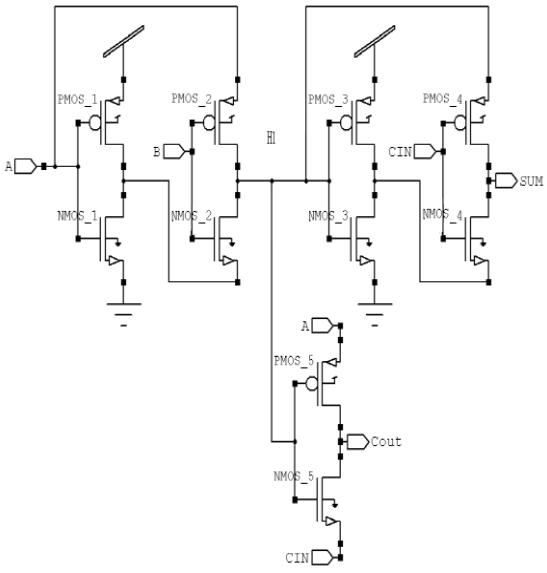

Fig. 4. 10T MGDI Full Adder

This design used Modified Gate Diffusion Input technique for generation of XOR function. XOR gate is implemented using the four transistors. The adder cell is implementing using the two XOR gates and one MUX. Figure 4 shows the Modified GDI full adder using 10 transistors. The figure has first XOR gate input terminal A and B and the output is H_1 (A XOR B). Output of the first XOR gate is connected to the one of the input of the second XOR gate. Second XOR gate output is generating the SUM (A XOR B XOR C_{in}). C_{out} is equal to A when H_1=0 and C_{out} is equal to C_{in} when H_1=1.

C. 9T MGDI Full Adder

In this section full adder design is implemented using the two different XOR gates and MUX. In the existing system the first XOR gate can be implemented with the help of three transistors. The three transistor XOR gate can be implemented with two PMOS transistor and one NMOS transistor. The second XOR gate can be implemented with the help of four transistors. The four transistor XOR gate can be implemented with two PMOS transistor and two NMOS transistor. The MUX gate is design using two transistor one NMOS and one PMOS transistor. This MGDI full adder design cell is implemented using the only 9 transistor. In the fig. 5 shown the 9T MGDI full adder.

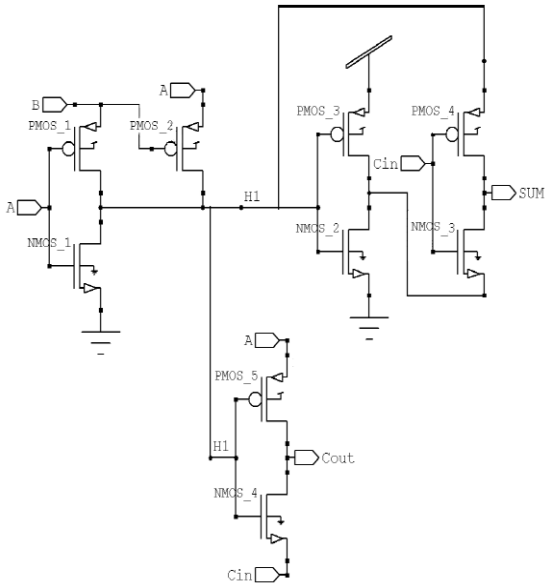

Fig. 5 9T MGDI Full Adder

D. 8T MGDI Full Adder

In this section full adder is also implemented using the two XOR gates and one MUX. In the existing system the XOR gates can be implemented with the help of three transistors. The three transistor XOR gate can be implemented with two PMOS transistor and one NMOS transistor using the modified GDI technique. In the fig. 6 shown the modified GDI full adder are used 8 transistors to circuit design. In the fig. 6 show the 3T first XOR gate output is H_1 (A XOR B). The output of first XOR gate is connected to the input of next XOR gate. The output of

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second XOR gate generates the SUM signal of full adder (A XOR B XOR C_{in}). The carry signal output C_{out} is equal to the input A when first XOR gate output H_1 is equal to the zero and carry signal output C_{out} is equal to the input C_{in} when first XOR gate output H_1 is equal to the one.

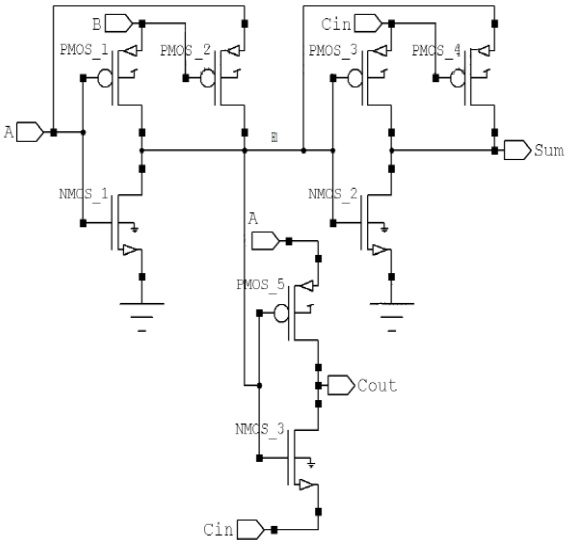

Fig. 6. 8T MGDI Full Adder

5. SIMULATION RESULT AND ANALYSIS

Design and simulation of four different Modified GDI full adders is implemented using Tanner EDA tool at 90nm technology with supply voltage varying from 0.8V to 1.6V. The performance of the modified GDI full adder such as 12T MGDI, 10T MGDI, 9T MGDI and 8T MGDI is analyzed in terms of the power consumption, delay, PDP and number of transistor count. The comparison of these four full adder designs in terms of delay, power and power delay product value is shown in table 3.

Table. 3. Power, Delay and PDP at 1.2v

Technique	Power	Delay	PDP
12T MGDI	91.24nW	9.459ns	0.86pJ
10T MGDI	1.317uW	5.272ns	6.94pJ
9T MGDI	0.627uW	9.988ns	6.27pJ
8T MGDI	61.14nW	81.21ps	4.96pJ

12T, 10T, 9T and 8T MGDI full adder is simulated and the output waveform at supply voltage 1.2V is shown in simultaneously figure 7, 8, 9, 10. For each transition the delay is measured from half of the rise time and fall time voltage swing. Fig. 11 shows the delay of all four MGDI full adders at different supply voltages. The 8T MGDI full adder has very low delay as compared to the other MGDI full adder. The average power consumption for all MGDI full adders under the varying supply voltage from 0.8V to 1.6V is shown in fig. 12. PDP is the product of the power and delay. It is important factor in low power functionality of any design. It is the quantitative measure for efficiency. The PDP with varying supply voltage is shown in fig. 13.

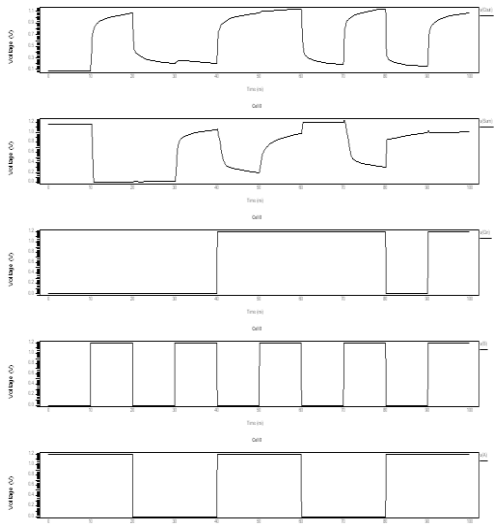

Fig. 7. Waveform of 12T MGDI full adder

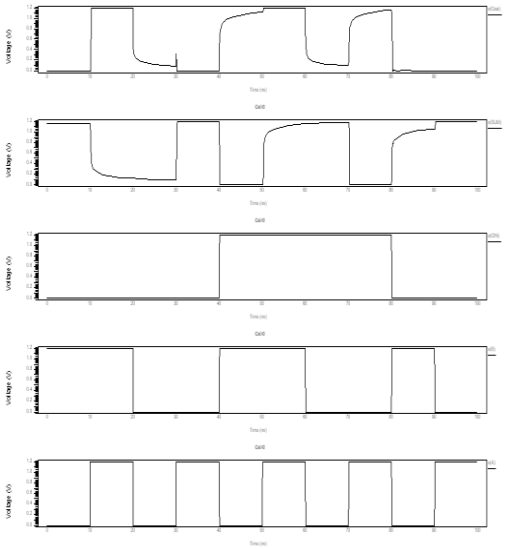

Fig. 8. Waveform of 10T MGDI full adder

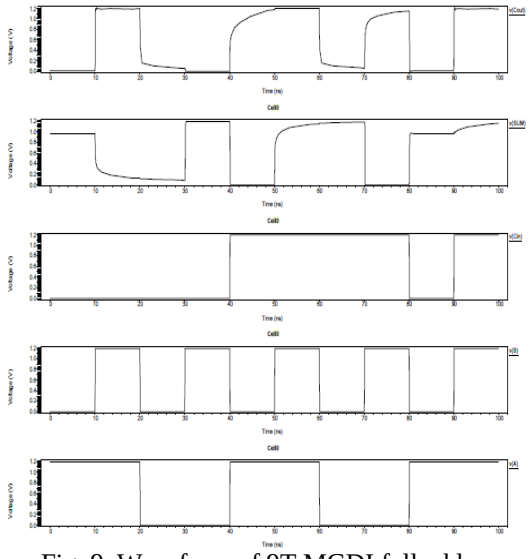

Fig. 9. Waveform of 9T MGDI full adder

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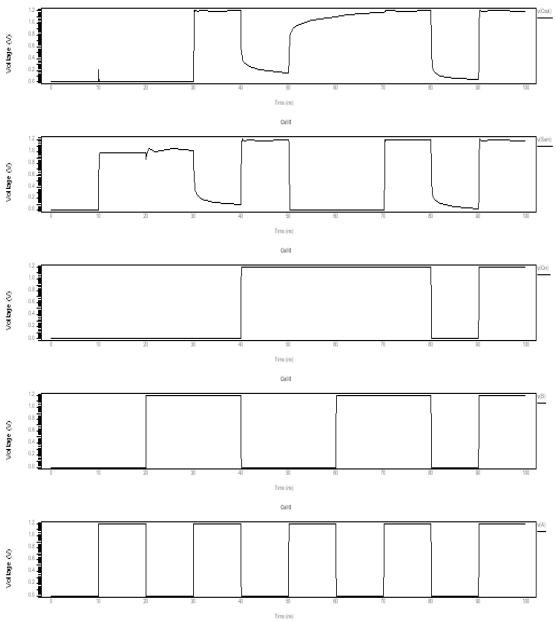

Fig. 10. Waveform of 8T MGDI full adder

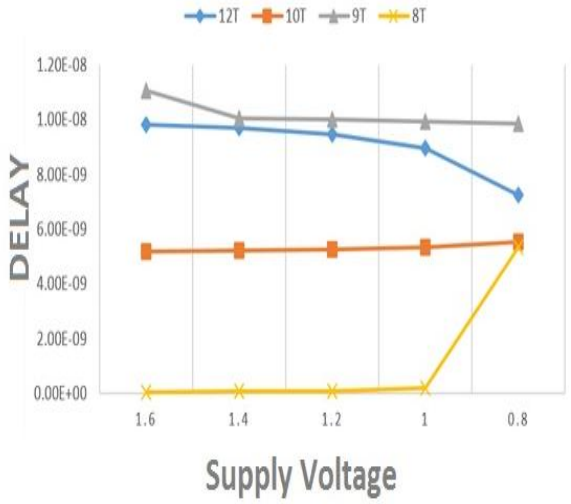

Fig. 11. Delay with respect to supply voltage

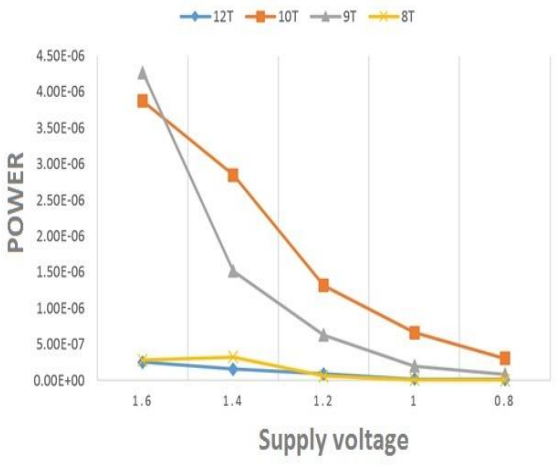

Fig. 12. Power with respect to supply voltage

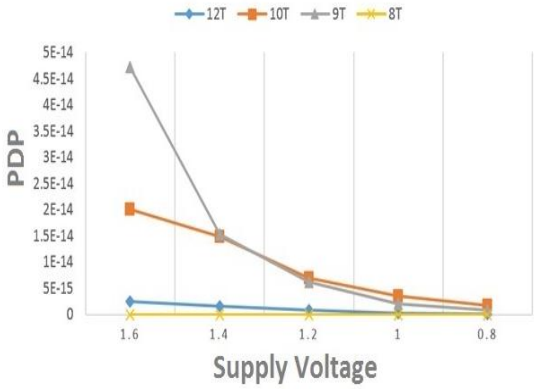

Fig. 13. PDP with respect to supply voltage

6. CONCLUSION

Four MGDI 1 bit full adder designs are presented in this paper. These full adder designs are successfully operated at low voltage having good driving capability. The 8T MGDI full adder has low power consumption, low delay and low power delay product as compared to the 12T full adder, 10T full adder and 9T full adder. The result shows that, among all the MGDI full adder design 8T MGDI full adder is best suited for low power application. The 8T full adder has minimum count of number of transistors. Reducing number of transistors used has resulted in a great reduction in switching activity and area. Also there is considerable reduction in power by minimizing static and dynamic power dissipation that overall helps to improve the speed of the design leading to the best PDP.

Performance analysis comparison of 8T, 10T, 9T and 12T MGDI full adder cell shows that 8T full adder is the best cell among the four full adder designs. Hence, the proposed cell can be used in designing of low power high speed embedded system memories.

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